Leakage Current Analysis

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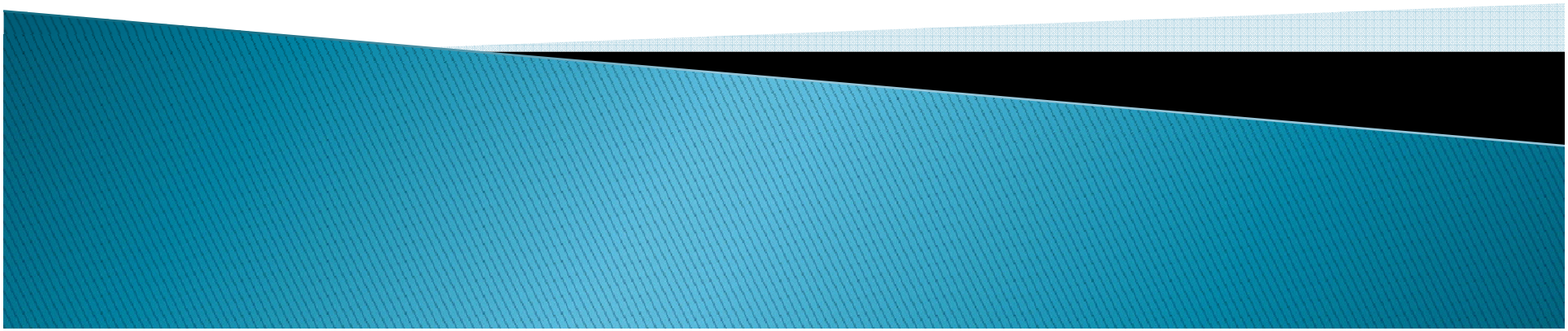
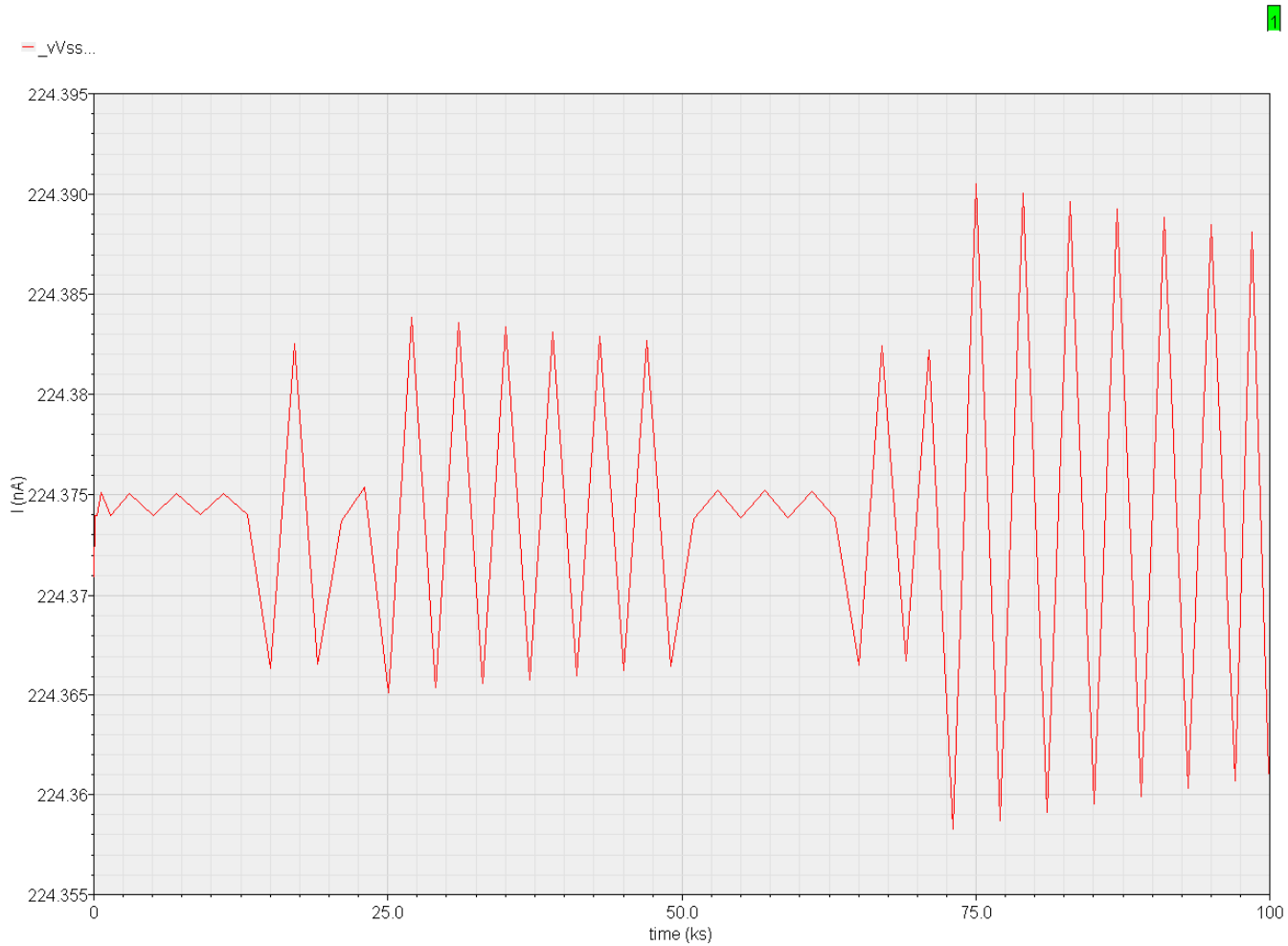
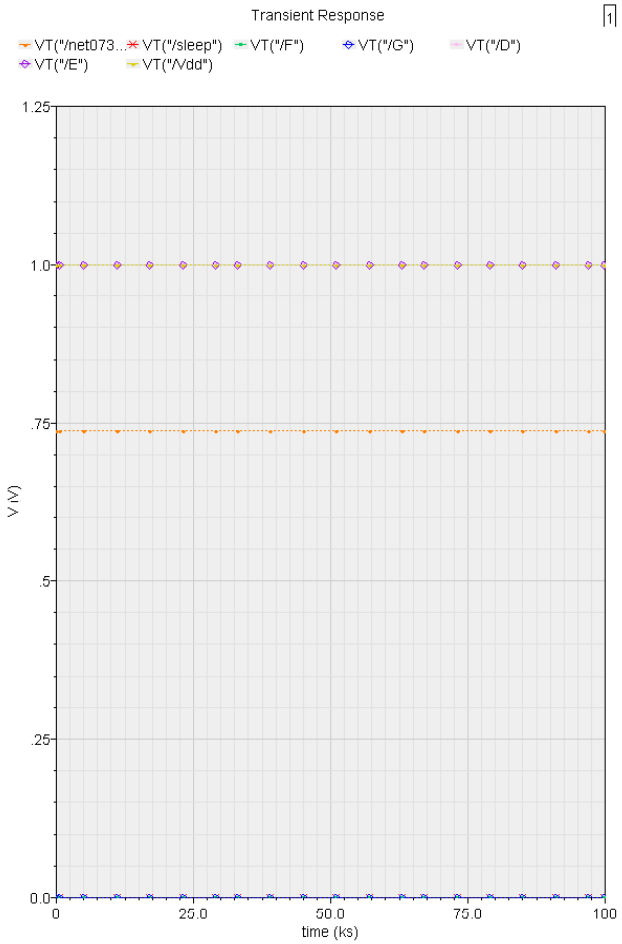
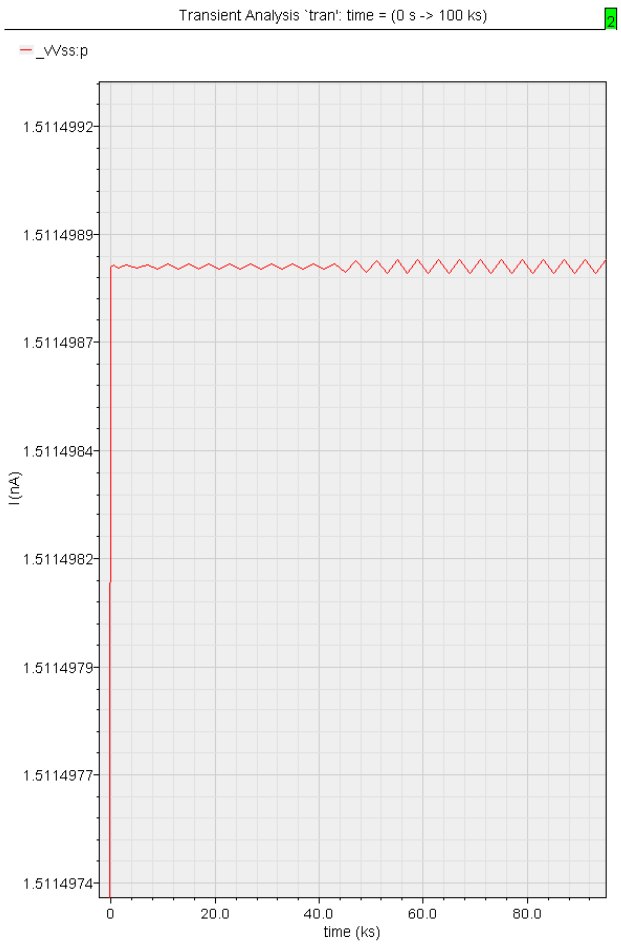


Leakage Current

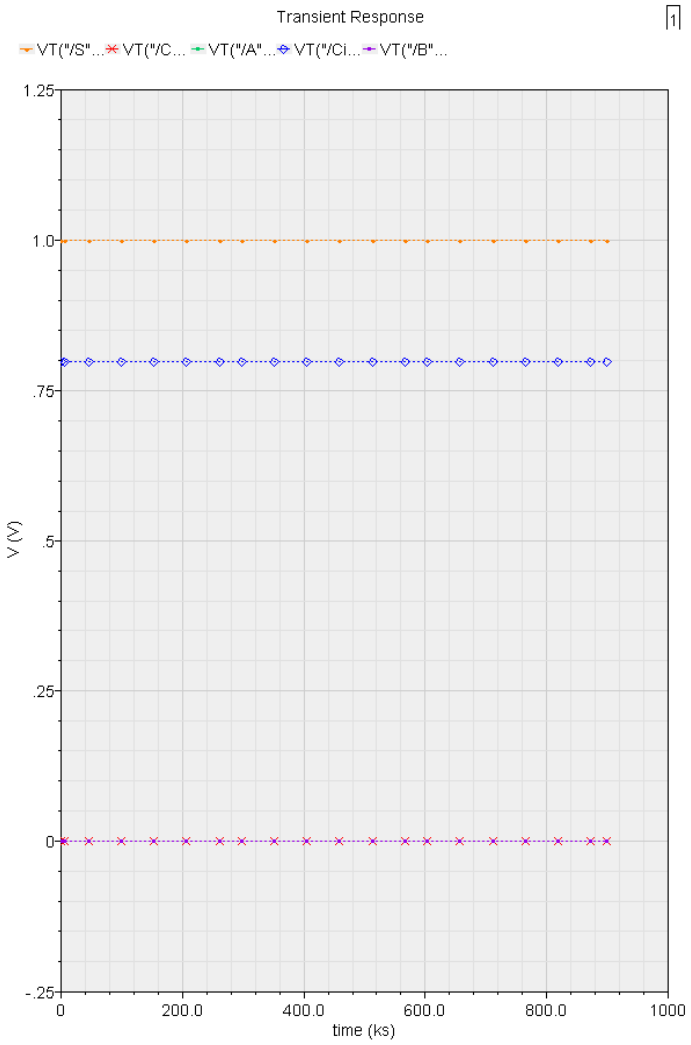


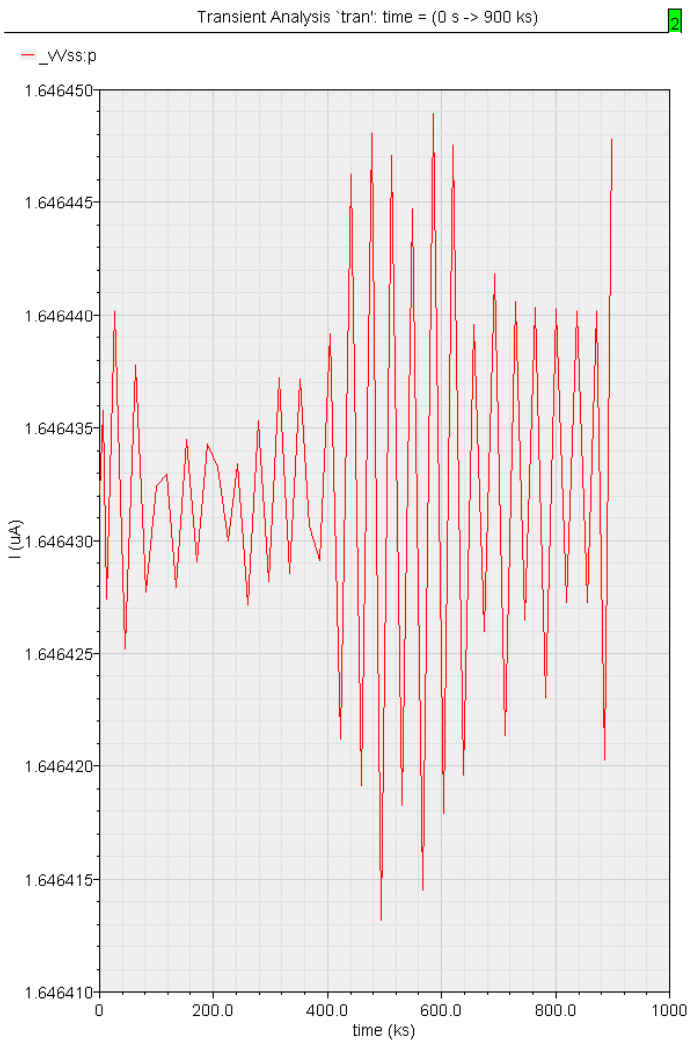
Power Gating





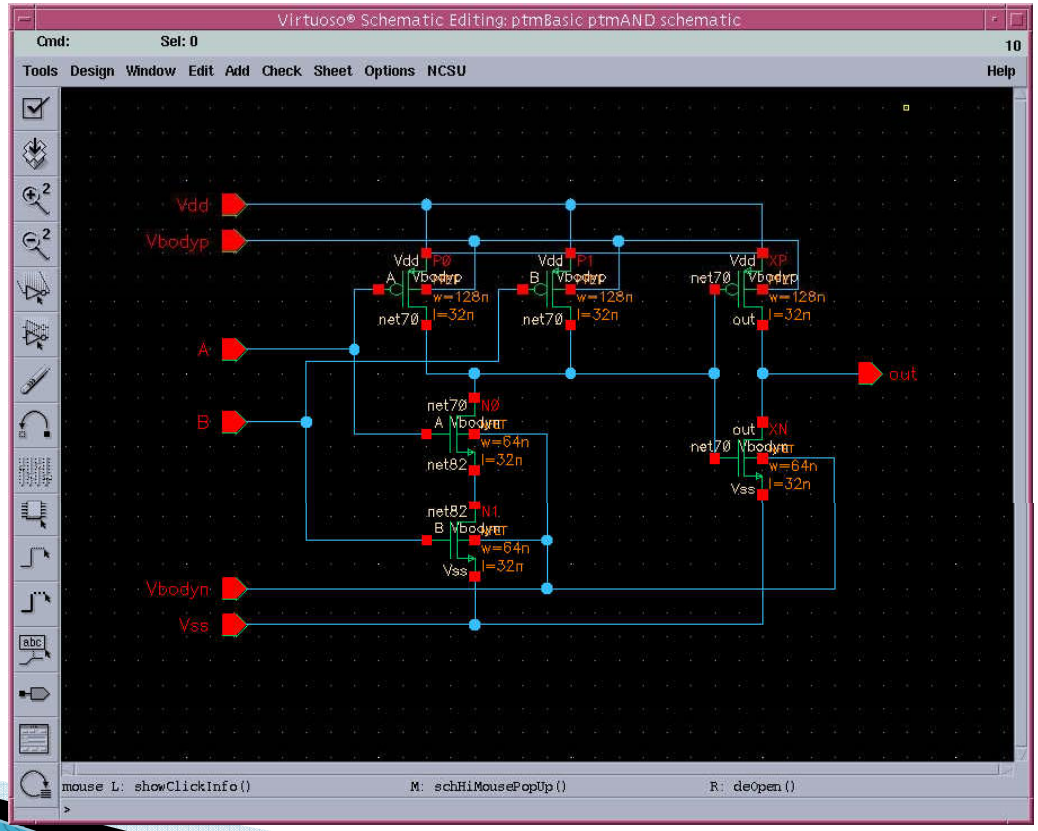
Input Vector Forcing





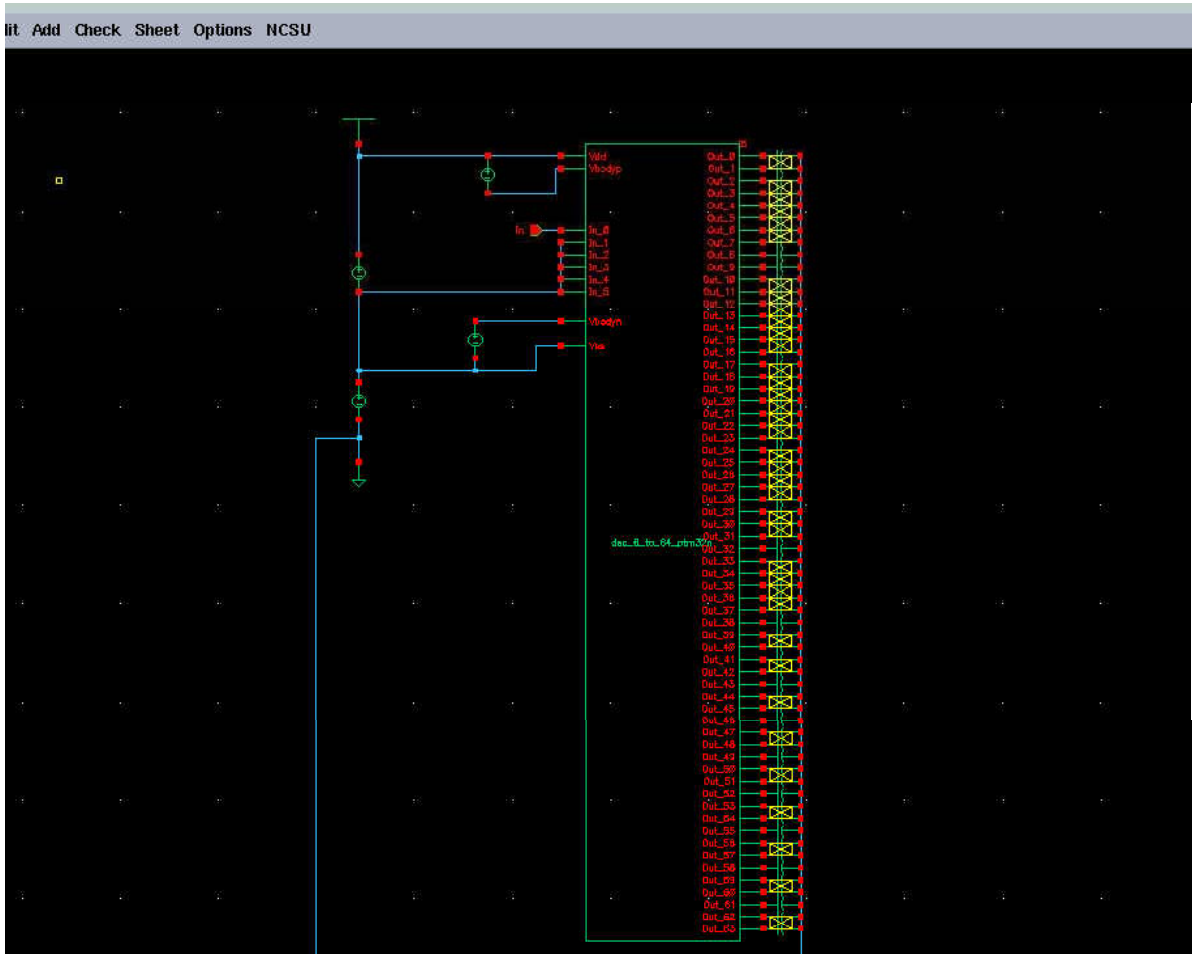
Body Bias

1. AND Gate – with body bias pins (32nm)



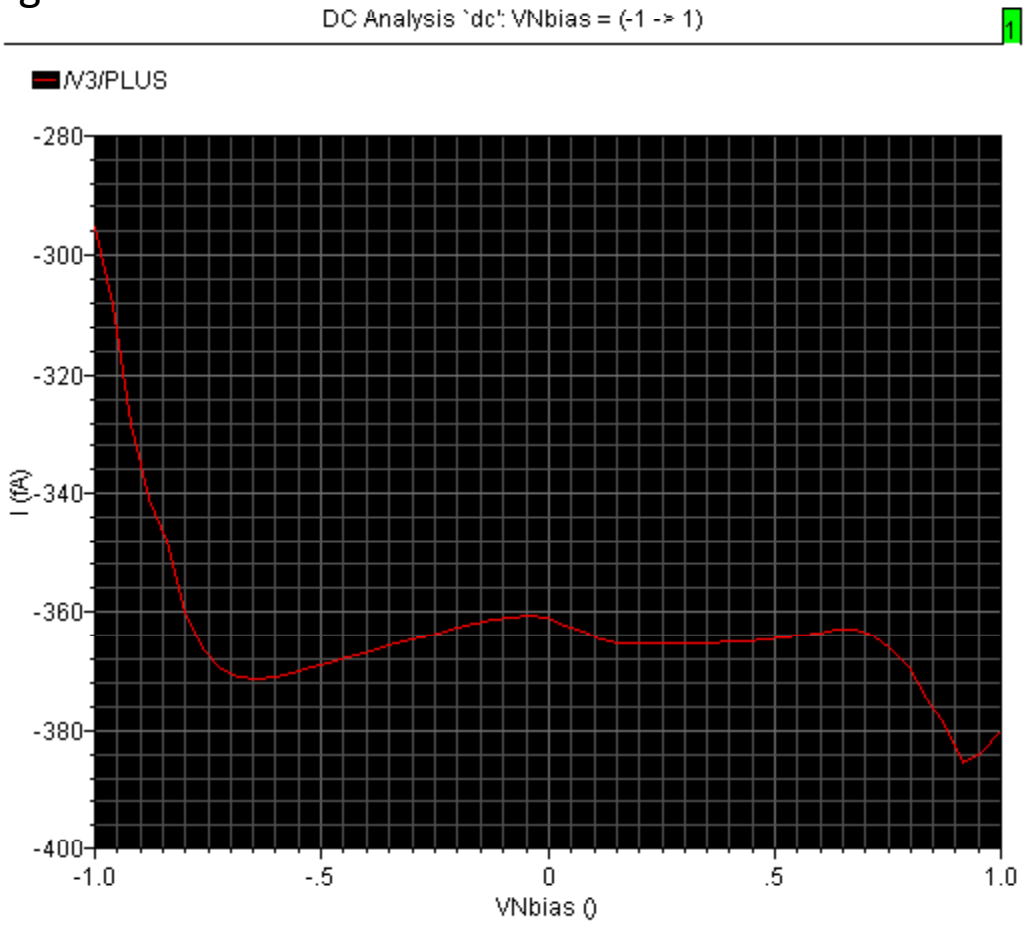
Body Bias

2. 6 bit to 64 bit Decoder – with body bias pins (32nm)

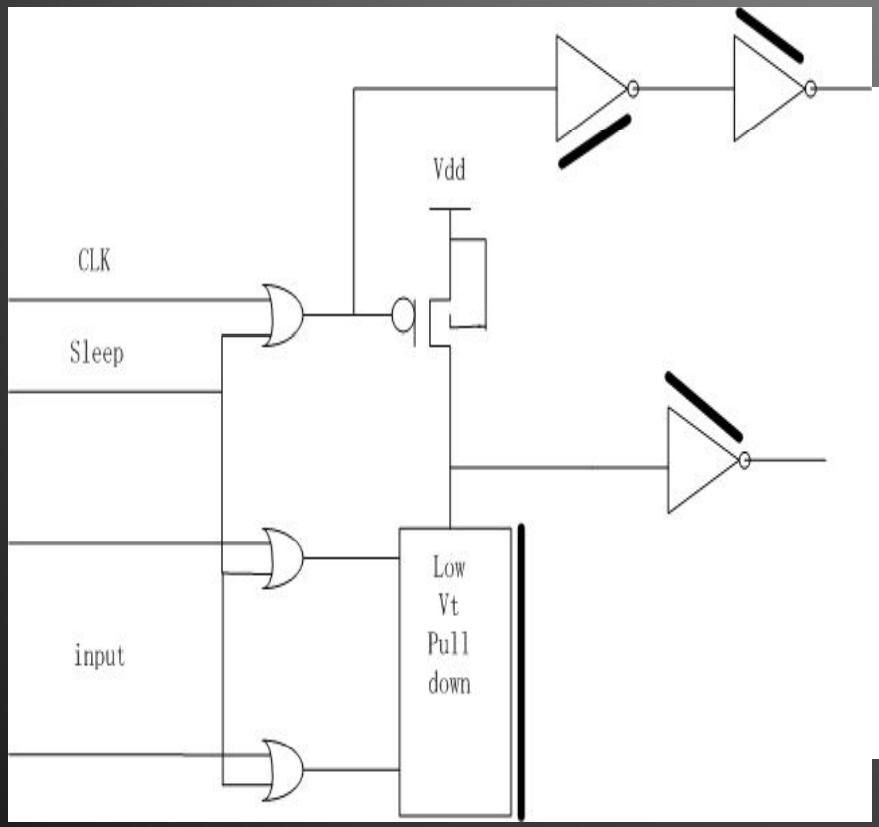


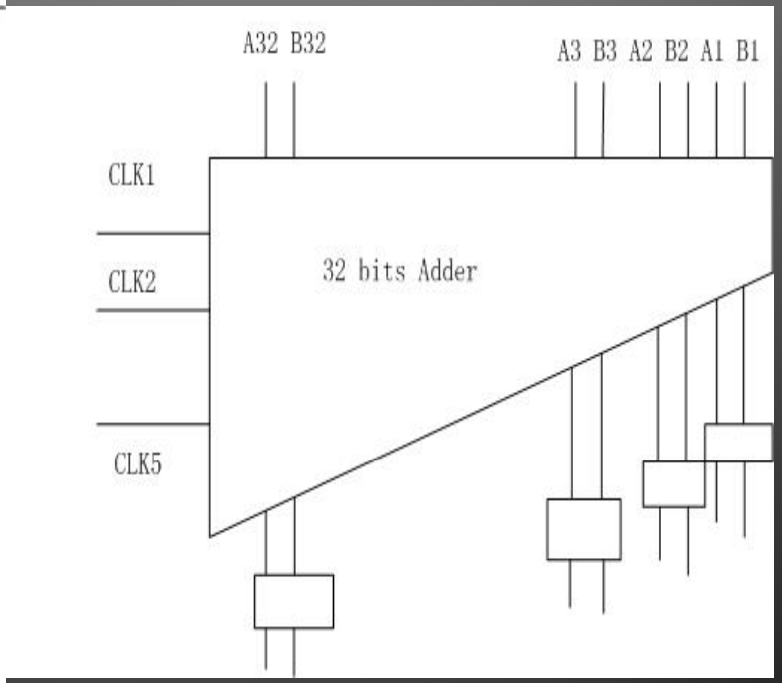
Body Bias

3. Decoder current leakage



Dual VT Dynamic Domino Logic

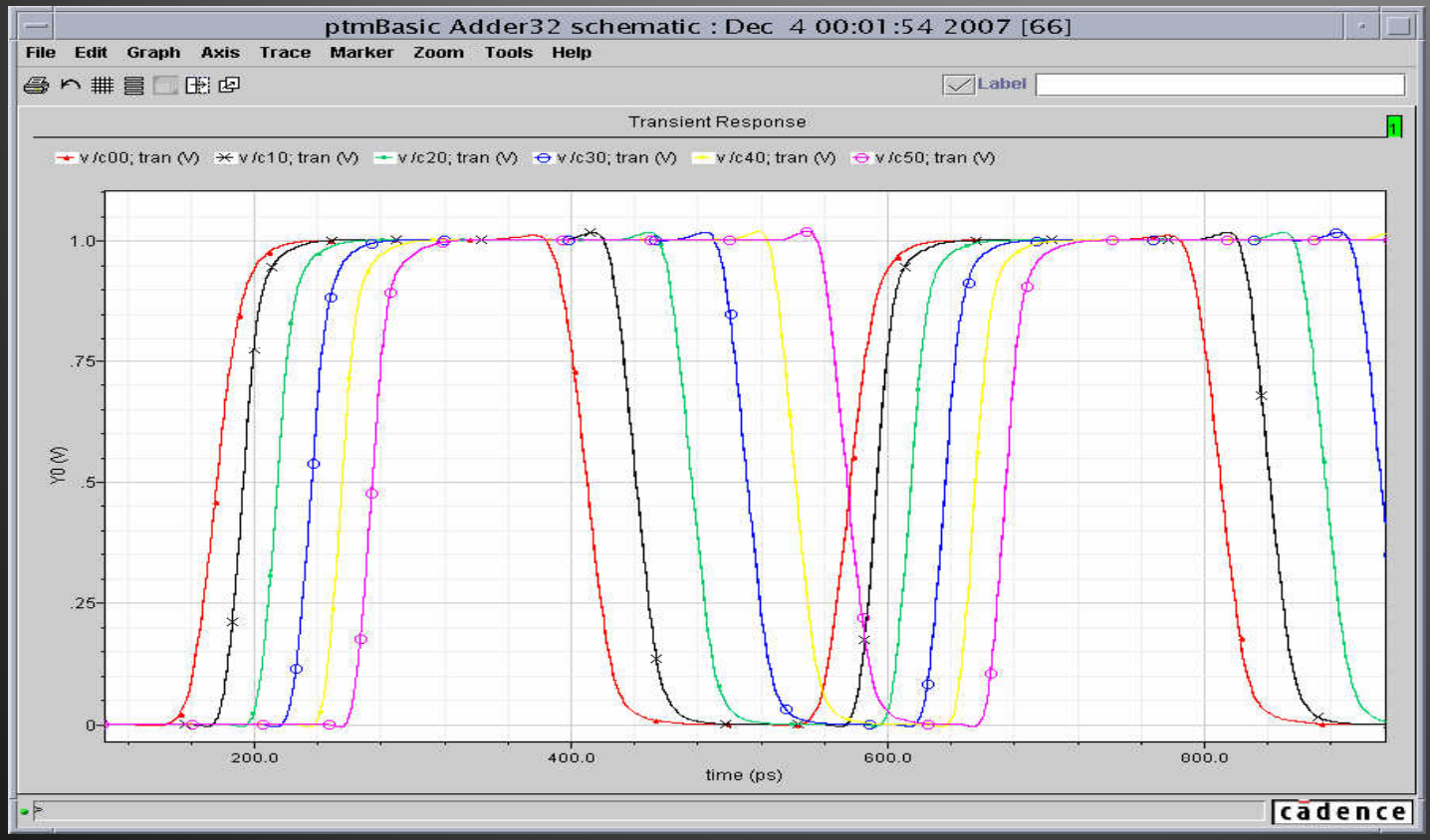




1. Use high VT Transistor during the precharge. Using Low Vt pulldown network.

2. During the stand by mode, all the internal inputs are set to minimize the leakage.

Dual VT Dynamic Domino Logic



1. Trade off the precharge time to have low leakage.

Simulation results and discussion

- 45nm Pw/Nw = 2.0

	Eva.	Pre.	Leakage input= 1	Leakage Input =0
HVT	40ps	29ps	32fA	1.2uA
LVT	24ps	17ps	300fA	53uA
DVT	22ps	28ps	270fA	39uA

32nm Pw/Nw =2.0

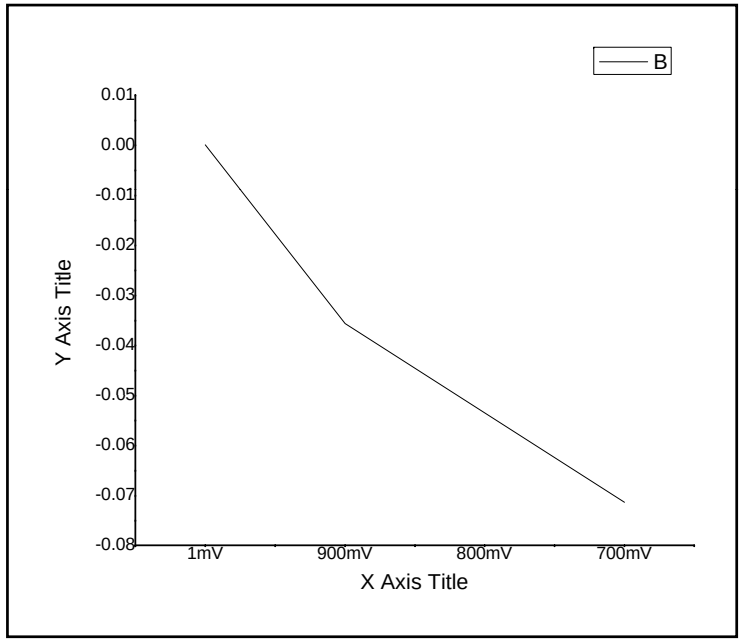
	Eva.	Pre.	Leakage input= 1	Leakage Input =0
HVT	32ps	26ps	45fA	1.8uA
LVT	18ps	13ps	430fA	66uA
DVT	17ps	26ps	360fA	54uA

1. DVT precharge is close to the HVT. DVT evaluation is faster than LVT.

2. Sizing is a big problem. The high Vt transistor should be small to cut off the leakage, but that will make the pre_delay worse.

3. I tried use PW/NW = 0.6, get the DVT leakage close to HVT, but with a large precharg

Forward Bias to reduce the precharge delay



Forward bias do not improve the precharge expansion very much.